REMARKS

Present Status of the Application

The Office Action mailed August 7, 2003 rejected all presently pending claims 1-20. Specifically, claims 1-20 were rejected under 35 U.S.C. 102(e) as being anticipated by Satoh et al (US 6,531,350). In response thereto, Applicants have amended independent claims 1, 2 and 12. Reconsideration of claims 1-20 is respectfully requested.

Summary of the Invention

This invention is directed to a method for fabricating a non-volatile memory. In the method, a strip stacked structure comprising a gate conductive layer and a charge trapping layer (or gate dielectric layer) is formed, and a buried drain line is formed beside the strip stacked structure to serve as a buried bit line. An insulating layer is formed on the buried drain line, and then a silicon layer and a cap layer is sequentially formed covering the strip stacked structure and the insulating layer. Thereafter, the cap layer, the silicon layer, and the strip stacked structure are patterned successively in a direction perpendicular to the buried drain line to form a stacked gate structure, wherein the patterned silicon layer serves as a word line. A liner layer is formed on the exposed surfaces of the silicon layer, the gate structures and the substrate, the cap layer is removed, and then a metal salicide layer is formed on the silicon layer.

Discussion of Office Action Rejections under 35 U.S.C. 102(e)

Rejection of Claim 1

As mentioned above, the features of this invention include at least: 1) a buried drain line as a buried bit line is formed beside a strip stacked structure; 2) a silicon layer and a cap layer are sequentially formed covering the strip stacked structure and the insulating layer on the buried drain line; 3) the cap layer, the silicon layer, and the strip stacked structure are patterned in a direction perpendicular to the buried drain line; and 4) the patterned silicon layer serves as a word line. The features can be supported by the specification and the drawings, and are recited in the amended claim 1 as follows, marked by underlines.

1. (Currently Amended) A method for fabricating a non-volatile memory, comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a dielectric layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a stacked gate structure, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

Satoh et al. fail to teach or suggest to form a buried drain ***as a buried bit line***. As described in col. 6, line 33, since the gate conductive layer 140 is called as a "word gate" and no additional word line is formed, the gate conductive layer 140 must serve as ***a word line perpendicular to the paper surface***. Therefore, the buried drain 103 ***cannot*** be a buried bit line ***perpendicular to the paper surface, otherwise memory cells cannot be defined***. That is, the buried drains in Satoh et al. must be separated from each other in X and Y directions.

Satoh et al. also fail to teach or suggest to form ***sequentially*** a silicon layer and a cap layer covering the strip stacked structure and the insulating layer on the buried drain line. As described in col. 6, line 52, the layer 127 is a ***silicon oxide layer***, but ***not a silicon layer*** as indicated by the Examiner. Moreover, ***the cap layer 130 must be formed first*** since it is located under the silicon oxide layer 127. Furthermore, as shown in FIG. 1N, the silicon oxide layer 127 and the cap layer 130 only cover the gate conductive layer 140, but not cover the insulating layer 124 on the buried drain 103 (there is no buried drain/bit line in Satoh et al.).

Satoh et al. also fail to teach or suggest to pattern the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line (there is no buried drain/bit line in Satoh et al.). In the related description of FIGs. 1A-1R, there is no description that the strip stacked structure is further patterned in this way. In fact, since the gate conductive layer 140 directly serves as a word line as mentioned above, the gate conductive layer 140 in the

strip stacked structure cannot be further patterned perpendicularly, ***otherwise the word line will be divided into fragments and cannot function as a word line.***

Furthermore, since no such a silicon layer is formed and patterned in Satoh et al. (the ***silicon layer*** indicated by Examiner is actually ***a silicon oxide layer***), the patterned silicon layer serving as a word line in this invention is also not taught or suggested by Satoh et al.

For at least the reasons mentioned above, Applicants respectfully submit that claim 1 is not anticipated by the cited prior art.

Rejection of Claims 2-11

The aforementioned features of claim 1 are also recited in independent claim 2 as follows, marked by underlines:

2. (Currently Amended) A method for fabricating a nitride read-only memory (NROM), comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a charge trapping layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a stacked gate structure, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

Satoh et al. fail to teach or suggest to form a buried drain as a buried bit line. As described in col. 11, line 8, since the gate conductive layer 240 is called as a "memory word gate" and no additional word line is formed, that the gate conductive layer 240 must serve as ***a word line perpendicular to the paper surface.*** Therefore, the buried drain 205 ***cannot*** be a buried bit line ***perpendicular to the paper surface, otherwise memory cells cannot be defined.***

That is, the buried drains in Satoh et al. must be separated from each other in X and Y directions.

Satoh et al. also fail to teach or suggest to form ***sequentially*** a silicon layer and a cap layer covering the strip stacked structure and the insulating layer on the buried drain line. As described in col. 11, line 64, the layer 226 is a ***silicon oxide layer***, but ***not a silicon layer*** as indicated by the Examiner. Moreover, as shown in FIG. 1N, the silicon oxide layer 226 and the cap layer 232 only cover the sidewall of the gate conductive layer 140, but not cover the insulating layer 243 on the buried drain 205 (there is no buried drain/bit line in Satoh et al.). On the contrary, it is the insulating layer 243 on the buried drain 205 that covers a portion of the cap layer 232.

Satoh et al. also fail to teach or suggest to pattern the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line. In the related description of FIGs. 2A-2R, there is no description that the strip stacked structure is further patterned in this way. In fact, since the gate conductive layer 240 directly serves as a word line as mentioned above, the gate conductive layer 240 in the strip stacked structure cannot be further patterned perpendicularly, ***otherwise the word line will be divided into fragments and cannot function as a word line.***

Furthermore, since no such a silicon layer is formed and patterned in Satoh et al. (the ***silicon layer*** indicated by Examiner is actually ***a silicon oxide layer***), the patterned silicon layer serving as a word line in this invention is also not taught or suggested by Satoh et al.

For at least the reasons mentioned above, Applicants respectfully submit that independent claim 2 is not anticipated by the cited prior art.

For at least the same reasons mentioned above, Applicants respectfully submit that claims 3-11 dependent from independent claim 2 are not anticipated by the cited prior art either.

Rejection of Claims 12-20

The aforementioned features of claim 1 are also recited in independent claim 12 as follows, marked by underlines:

12. (Currently Amended) A method for fabricating a read-only memory, comprising:

providing a substrate having a strip stacked structure thereon, wherein the strip stacked structure comprises a gate conductive layer and a gate dielectric layer under the gate conductive layer;

forming a buried drain line as a buried bit line in the substrate beside the strip stacked structure;

forming an insulating layer on the buried drain line;

forming sequentially a silicon layer and a cap layer over the substrate covering the strip stacked structure and the insulating layer;

patterning the cap layer, the silicon layer, and the strip stacked structure in a direction perpendicular to the buried drain line to form a stacked gate structure, wherein the patterned silicon layer serves as a word line;

forming a liner layer on exposed surfaces of the silicon layer, the gate structures and the substrate;

removing the cap layer; and

forming a metal salicide (self-aligned silicide) layer on the silicon layer.

At first, Applicants respectfully point out that the layer 126 in FIG. 1D is not a gate dielectric layer as indicated by Examiner, while the gate dielectric layer should be the layer labeled with "120" in FIG. 1D.

Satoh et al. fail to teach or suggest to form a buried drain as a buried bit line. As described in col. 6, line 33, since the gate conductive layer 140 is called as a "word gate" and no additional word line is formed, the gate conductive layer 140 must serve as ***a word line perpendicular to the paper surface***. Therefore, the buried drain 103 ***cannot*** be a buried bit line ***perpendicular to the paper surface, otherwise memory cells cannot be defined***. That is, the buried drains in Satoh et al. must be separated from each other in X and Y directions.

Satoh et al. also fail to teach or suggest to form ***sequentially*** a silicon layer and a cap layer covering the strip stacked structure and the insulating layer on the buried drain line. As described in col. 6, line 52, the layer 127 is a ***silicon oxide layer***, but ***not a silicon layer*** as indicated by the Examiner. Moreover, ***the cap layer 130 must be formed first*** since it is located under the silicon oxide layer 127. Furthermore, the silicon oxide layer 127 and the cap layer 130 only cover the gate conductive layer 140, but not cover the insulating layer 124 on the buried drain (there is no buried drain/bit line in Satoh et al.).

Satoh et al. also fail to teach or suggest to pattern the cap layer, the silicon layer, and the

strip stacked structure in a direction perpendicular to the buried drain line. In the related description of FIGs. 1A-1R, there is no description that the strip stacked structure is further patterned in this way. In fact, since the gate conductive layer 140 directly serves as a word line as mentioned above, the gate conductive layer 140 in the strip stacked structure cannot be further patterned perpendicularly, ***otherwise the word line will be divided into fragments and cannot function as a word line.***

Furthermore, since no such a silicon layer is formed and patterned in Satoh et al. (the ***silicon layer*** indicated by Examiner is actually ***a silicon oxide layer***), the patterned silicon layer serving as a word line in this invention is also not taught or suggested by Satoh et al.

For at least the reasons mentioned above, Applicants respectfully submit that independent claim 12 is not anticipated by the cited prior art.

For at least the same reasons mentioned above, Applicants respectfully submit that claims 13-20 dependent from independent claim 12 are not anticipated by the cited prior art either.

CONCLUSION

For at least the forgoing reasons, it is believed that pending claims 1-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 10/16/2003

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809